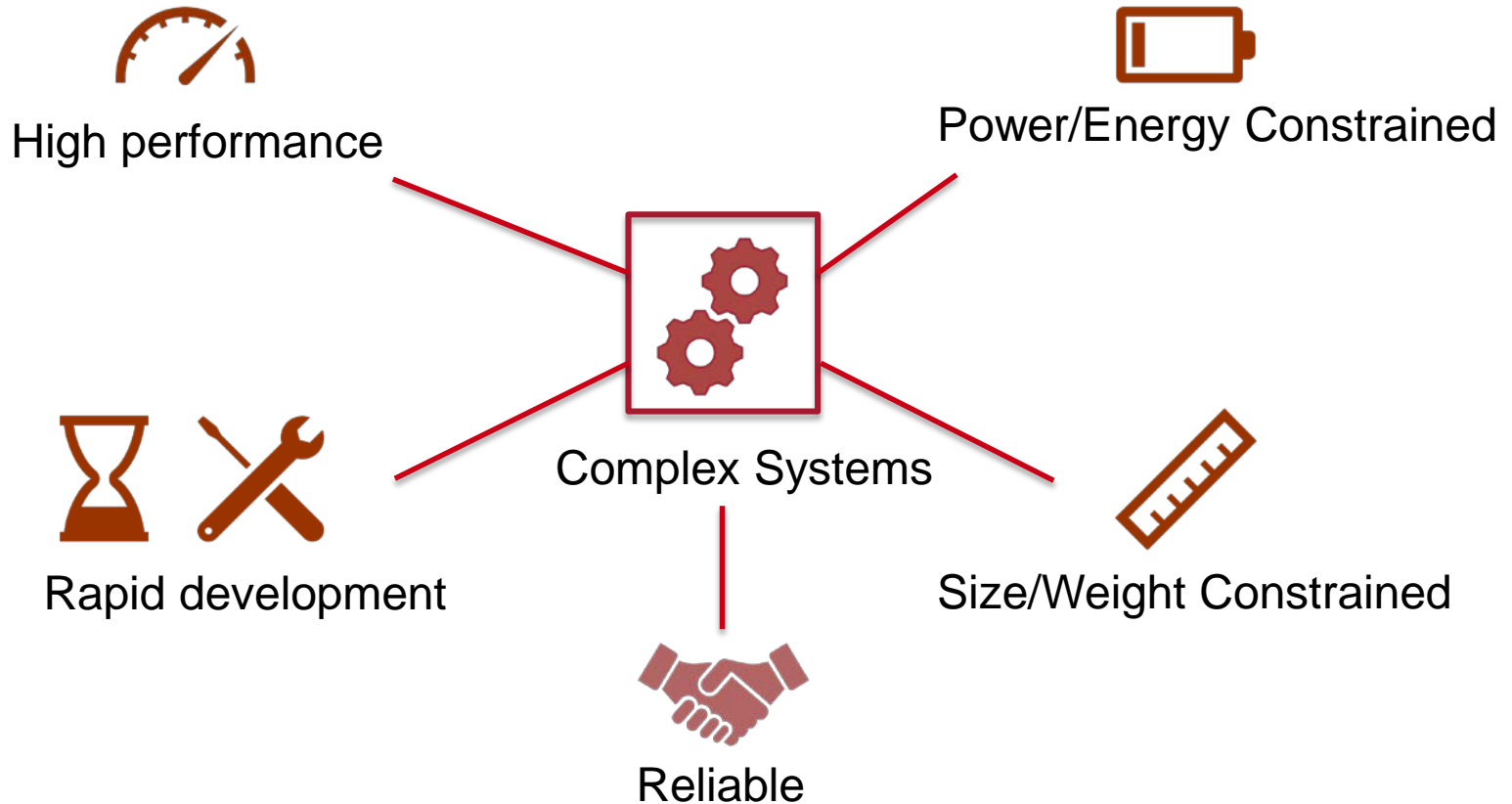


Towards Reliable FPGA-based Reconfigurable Satellite Systems

Ediz Cetin
School of Engineering

Email: ediz.cetin@mq.edu.au

CubeSat Digital Processing Requirements



MACQUARIE
University

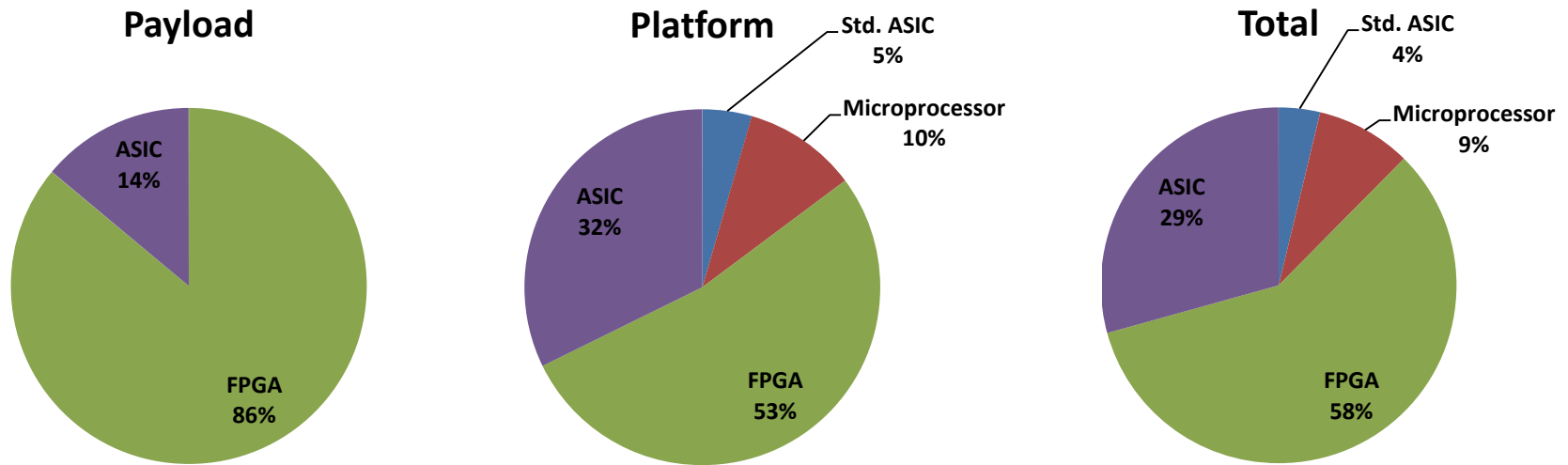
We develop design methods for highly reliable
FPGA-based digital systems in space



UNSW
SYDNEY

FPGAs in Space: ESA Sentinel 2 Mission

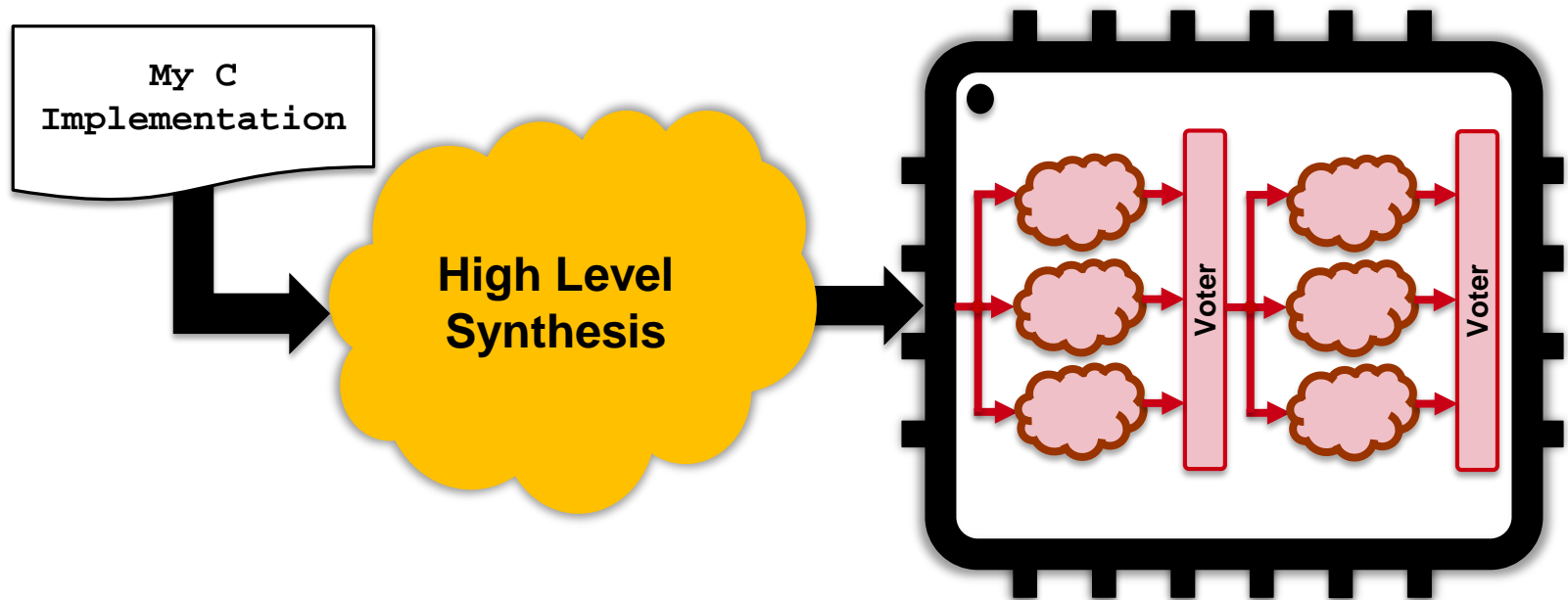
Field Programmable Gate Arrays (FPGAs) have high performance, low power consumption, low non-recurring engineering costs and flexibility



IC Type	Quantity Platform	Quantity Payload
FPGA	118	37
Custom ASIC	72	6
Microprocessor	23	0
Standard ASIC	10	0

From C to Fault Tolerant FPGA Implementation

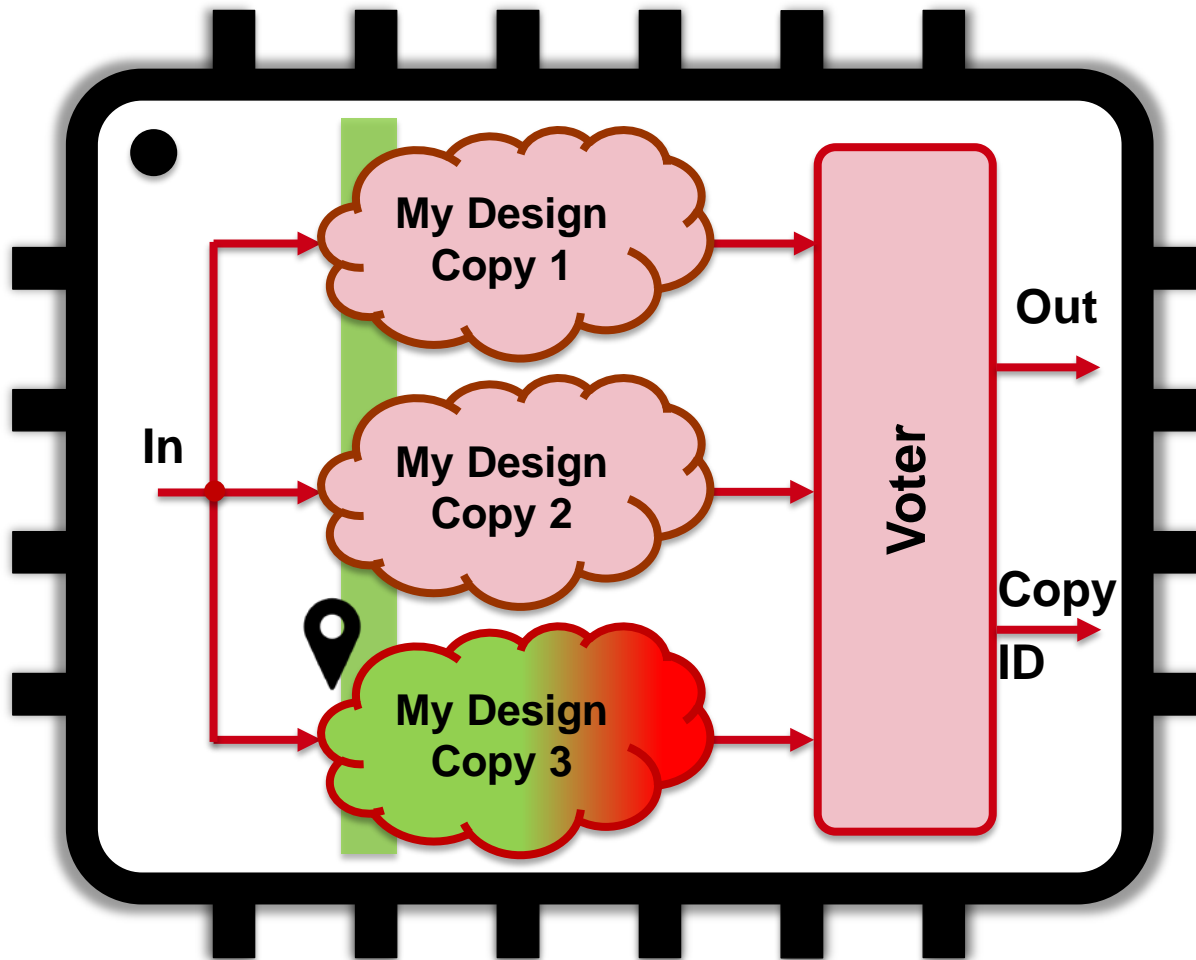
- **TLegUp** – Given high level C code, generates low level highly reliable FPGA implementations that are already triplicated and ready to deploy on FPGAs



See: Agiakatsikas *et. al*, "From C to Triple Modular Redundant Circuits - An Automated Flow", *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 2018.

Lee *et. al*, "TLegUp: A TMR Code Generation Tool for SRAM-Based FPGA Applications Using HLS", *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'17)*, May 2017. DOI: 10.1109/FCCM.2017.57

FPGA Fabric and SEUs – Hybrid Frame and Module Based Error Recovery (FMER)



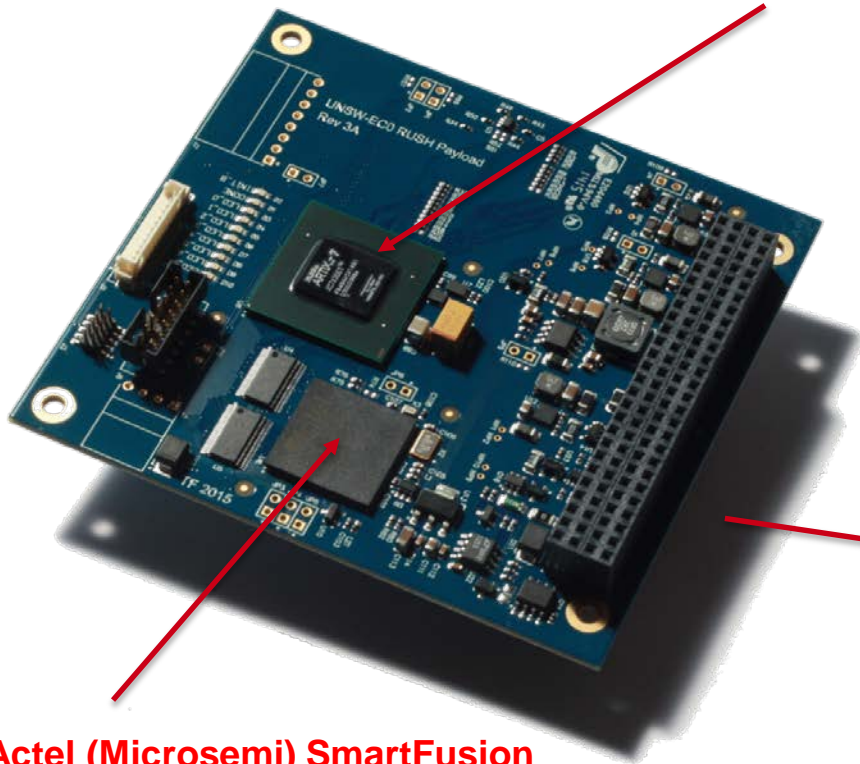
For a 2-year LEO Mission
(Using 11 CHStone
benchmark circuits):

- System availability (# of 9s):
☹️ FMER (9), Scrubbing (9)
- Energy Saving (relative to
Scrubbing):
😊 60%

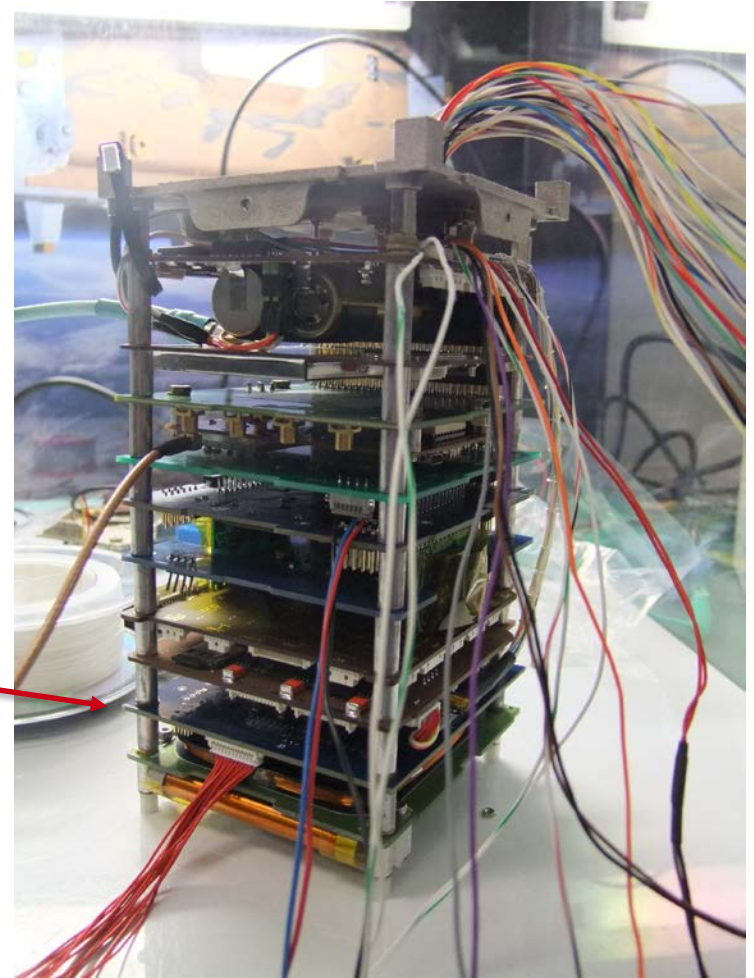
RUSH Platform

“Rapid recovery from SEUs in reconfigurable hardware”

Xilinx Artix 7 SRAM-FPGA



Actel (Microsemi) SmartFusion
Flash-FPGA



UNSW-EC0

Projects and Launch Plans



RUSH

July 2018



RUSH

Late 2018



**Sounding
Rocket**

RUSH-DSP

Mid - Late 2019



Serpens-II

RUSH-SDR/OBC

Late 2019



Exiting Times Ahead !!!!

